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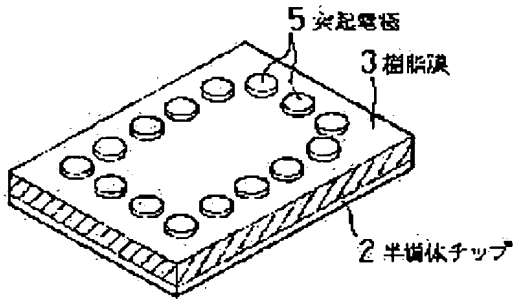
(54) SEMICONDUCTOR DEVICE

(57) Abstract:
PURPOSE: To improve handling operability of a semiconductor chip in a manufacturing step while reducing in thickness of the chip itself irrespective of the size of a semiconductor wafer and to obtain a small-sized thin semiconductor device.
CONSTITUTION: A semiconductor wafer 1 is reduced in thickness while forming a resin film 3 in a protective reinforcing plate, protrusion electrodes 5 protrude from the film 3 on a semiconductor chip 2 as an external connection terminal, and the film 3 is so cut as to be the same in size as the chip 2. Thus, a semiconductor device having high reliability, easy handling, small size and thickness, is obtained.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by the side face and the inferior surface of tongue of a semiconductor chip being exposed, the resin section which has the almost same size as this being formed in the aforementioned semiconductor chip top, and the salient electrode protruding from the top of the aforementioned resin section.
[Claim 2] A semiconductor device given in the patent claim 1 characterized by forming the insulation-protection strengthening layer in the principal piece on the front face of the maximum of the aforementioned resin section.
[Claim 3] The manufacture technique of a semiconductor device given in the patent claim 1 characterized by making the semiconductor wafer rear-face section remove, using as a protection strengthening plate the resin section under which the aforementioned salient electrode was laid.
[Claim 4] The manufacture technique of a semiconductor device given in the patent claim 1 characterized by forming an insulation-protection strengthening layer in a resin **** front face and a disconnection field front face, and cutting a disconnection field after exposing the disconnection field of a salient electrode point and a semiconductor wafer from the aforementioned resin section.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] this invention relates to the semiconductor device which makes the salient electrode point formed on the pad electrode layer of a semiconductor chip with an external end-connection child.
[0002]
[Description of the Prior Art] The grinding of the semiconductor wafer which pattern formation generally completed is carried out to predetermined thickness using a rear-face grinding method. This rear-face grinding method is grinding and a thing to remove about a semiconductor wafer side by **** by which ** ON of the diamond grain was carried out into the resin, pressurizing a semiconductor wafer uniformly and making [stick on the pattern side of a semiconductor wafer the elasticity nature film which makes the chloroethylene used as a protection film etc. a base material,] it rotate from on an elasticity film.
[0003] And the scribe line of the semiconductor wafer by which grinding was carried out was cut, it divided into each semiconductor chip, the semiconductor chip and the external terminal lead were mutually joined electrically through the bonding wire or TAB lead, and it was the technique with the common thing of carrying out manipulation formation of the external terminal lead after a resin seal.
[0004] Moreover, barrier metal membranes, such as Cr, were formed in behind, and Au bump was made to form in it alternatively with Au electrolysis plating, before carrying out the grinding of the semiconductor wafer side by the describing [above] rear-face grinding method and removing it, in order to make salient electrodes, such as Au bump, form on a semiconductor wafer.
[0005]
[Problem(s) to be Solved by the Invention] The semiconductor device is carried in all devices, such as a computer, a work station, a personal computer, a word processor, a cellular phone, and a small pocket camcorder, so much. In recent years, development of a miniaturization of these devices and lightweight-izing is remarkable, and since a miniaturization of these devices, lightweight-izing and highly-efficient-izing, and highly efficient-ization progress further, the demand to a miniaturization of the semiconductor device carried in these devices, the formation of thin type, and high-reliability-izing will be predicted to be what increases at an increasing tempo together with a demand called high integration of a semiconductor device, and highly-efficient-izing from now on. However, in connection with development of diameter[of the macrostomia]-izing of a semiconductor wafer, a limitation arises to make thickness thin by constraint called crash prevention of the semiconductor wafer at the time of a handling or grinding, as a result, the semiconductor chip contained to a semiconductor device becomes thick, and thin type-ized ****** of a semiconductor device has become the factor which checks thin type-ization of a device at the manipulation of semiconductor wafer ** by the conventional rear-face grinding method. Furthermore, as for the semiconductor wafer, it was common to have formed Au bump after rear-face grinding, in order to avoid a crash of the semiconductor wafer by the load concentration to Au bump at the time of rear-face grinding, and performing rear-face grinding, after forming Au bump had a possibility that it might be accompanied by extraordinary difficulty, when it took into consideration avoiding a crash of the semiconductor wafer by local concentration of a load.
[0006] On the other hand, the component-side product which the semiconductor device within a

device occupies It is in the orientation which increases in connection with high integration of a semiconductor device, and highly-efficient-izing. especially The inside of the conventional semiconductor device needs electric flow paths, such as a bonding wire and an inner lead. A component-side product essentially [since the outer lead for obtaining a junction is needed for the outside of a semiconductor device] becomes large. and further It had become the factor which the package height which consists of resin thickness and semiconductor chip thickness also becomes high, and these things check a miniaturization of a semiconductor device, and lightweight-ization, as a result checks a miniaturization of a device, and lightweight-ization.

[0007] Furthermore, the element side of the semiconductor chip divided after grinding tended to receive trauma simply according to few force from the exterior, and needed careful cautions for the handling of the semiconductor chip in an erector degree or a package process, or the setup of equipment conditions.

[0008] this invention aims at making into the minimum the thing the trauma to the element side of a semiconductor chip is made not to produce as soon as it is made not to be generated by semiconductor wafer crash, even if it processes a semiconductor wafer thinly by rear-face grinding, and a two-dimensional electric flow path, and making a component-side product small, and making resin thickness and semiconductor chip thickness into the minimum, and making a package height small.

[0009]

[Means for Solving the Problem] If the semiconductor device of this invention solves the above technical probrems and the schema is explained, it is as follows. Namely, using as a protection strengthening plate the resin section which laid underground the salient electrode which serves as an external end-connection child, carry out the grinding of the semiconductor wafer rear-face section, and a semiconductor wafer is made thin. After exposing the scribe line of a salient electrode point and a semiconductor wafer from this resin section and forming an insulation-protection strengthening layer in the principal piece of a resin **** front face, and a scribe line section front face, cut a scribe line and a semiconductor device is made to constitute. It constitutes so that that the salient electrode which protruded from the top of the resin section of this semiconductor device upper part is electric as an external end-connection child, and a mechanical junction may be obtained.

[0010]

[Function] Even if it processes a semiconductor wafer thinly by rear-face grinding, in order that the resin section formed on the semiconductor wafer may function as a protection strengthening plate according to the above-mentioned means, while the semiconductor wafer crash at the time among rear-face grinding of a handling is avoidable, a handling of the semiconductor chip in the raise in basic wages status in an erector degree or a package process is lost, and can also avoid the trauma to the element side of a semiconductor chip. Moreover, the semiconductor device of small [which the two-dimensional electric flow path was easily made / small / into the minimum, and made thin resin thickness and semiconductor chip thickness], and a thin shape can be formed by protruding the salient electrode which is made to become almost the same about the size of the resin section of the semiconductor device upper part, and the size of a semiconductor chip, and serves as an external end-connection child from the top of the resin section formed in the upper part of the aforementioned semiconductor device.

[0011]

[Example] The 1st example of this invention is explained based on the drawing 1 and the drawing 2 . Drawing 1 is a perspective diagram showing the semiconductor device of the 1st example of this invention, and drawing 2 is a cross section explaining the manufacture technique of the semiconductor device of the 1st example. After drawing 1 shows the status that the semiconductor wafer 1 in which the resin layer 3 and the salient electrode 5 were formed on the front face was cut in the size of each semiconductor chip 2, it performs grinding for the rear face of the semiconductor wafer 1 in the shape of a mirror plane using a rear-face grinding method where the resin layer 3 is formed in a front face before a disconnection, and it processes the thickness of the semiconductor wafer 1 thinly, it is cutting the scribe line 4 using a dicing blade. The grinding of the rear face of this semiconductor wafer 1 by making the resin layer 3 form on the front face of the semiconductor

wafer 1 before rear-face grinding The resin layer 3 is operated as a protection strengthening plate, and that whose thickness at the time of a wafer process manipulation is about 0.6mm if it is the semiconductor wafer 1 of the diameter of 6 inch can process the thickness of the semiconductor wafer 1 thinly to 0.35mm - about 0.4mm by the rear-face grinding method. Even if it is the semiconductor wafer 1 of the diameter of 8 inch, that whose thickness at the time of a wafer process manipulation is about 0.7mm can process the thickness of the semiconductor wafer 1 thinly to 0.4mm - about 0.5mm similarly. It can **, if it is not concerned in the thickness of the semiconductor wafer 1, i.e., the size of the semiconductor wafer 1, how but the thickness of the semiconductor wafer 1 is thinly processed by this. Here, the technique of making it heat-harden, after carrying out spin coating of the polyimide resin which uses the polyimide resin which has for example, low stress and high thermal resistance for the resin material which forms this resin layer 3, and is generally well used for the formation technique of the resin section is used. Moreover, in order to obtain a predetermined resin thickness, it is easily obtained by repeating spin coating. In addition, as a resin material of the resin layer 3 formed in the front face of the semiconductor wafer 1, it will also be possible to use the resin of the epoxy system which has low stress and low shrinkage characteristics instead of the above polyimide resins, the thickness of the predetermined resin layer 3 can be easily obtained by using the squeegee printing method, and, as a result, the function as a protection strengthening plate of the resin layer 3 will improve further.

[0012] The manufacture technique of the semiconductor device of the 1st example of this invention is explained based on drawing 2 . First, in the 1st process, as shown in drawing 2 A, on the electrode pad of the semiconductor wafer 1 which has the thickness which is about 0.6mm in which the pattern was formed, Au plating is alternatively given with electrolysis plating through a chromium thin film, and the circular cylinder-like salient electrode 5 is formed in the height of about 100 micrometers. Next, in the 2nd process, as shown in drawing 2B , the resin layer 3 is formed for the upper-limit section of the salient electrode 5 by the thickness about a wrap on the semiconductor wafer 1. And at the 3rd process, as shown in drawing 2 C, the grinding of the rear face of the semiconductor wafer 1 is carried out by the rear-face grinding method, using this resin layer 3 as a protection strengthening plate and adhesives, and the thickness of the semiconductor wafer 1 is thinly processed so that it may be set to about 0.4mm. At the 4th process, as shown in drawing 2 D, the top of the resin layer 3 established in the upper part of the semiconductor wafer 1 is etched lightly, and the upper-limit section of the salient electrode 5 is exposed. The resin layer 3 of the scribe line 4 is shaved off with a dicing blade, and the silicon-nitride layer 6 is made to form alternatively except for the upper-limit section of the salient electrode 5 by the plasma CVD method after elevated-temperature xeransis at the 5th process, as shown in drawing 2 E. Finally, at the 6th process, as shown in drawing 2 F, this semiconductor wafer 1 is stuck on the adhesive tape (not shown) for dicing, the semiconductor wafer 1 is completely shaved off with a dicing blade with the scribe line 4, and it separates into the one piece one semiconductor chip 2. In addition, in order to remove the resin layer 3 of the scribe line 4, not only the physical technique that was explained at the 5th process but the technique by chemical etching is possible. It is also possible for formation of the silicon-nitride layer 6 to perform it immediately after light etching of the resin layer 3 on the other hand, although the function as insulating strengthening protection falls a little.

[0013] Furthermore, the semiconductor device cut down by the size of each semiconductor chip 2 as mentioned above in drawing 1 The resin layer 3 is formed in the top of a semiconductor chip 2 which rear-face grinding is given and became thin as already explained. From the top of this resin layer 3, the point of the salient electrode 5 of the shape of a circular cylinder perpendicularly formed to the pad electrode of a semiconductor chip 2 has projected, the salient electrode 5 is an Au electrode formed using electrolysis plating, and the height is 80 micrometers - 100 micrometers. However, the configuration of this salient electrode 5 may be a circular cylinder-like, and may be a prism-like. On the other hand, the amount of vegetation of this salient electrode 5 is determined from the height of the salient electrode 5, the thickness of the resin layer 3, and a junction stability, and is making about 20 micrometers project in the 1st example. Moreover, in the 1st example, it has exposed, where the dicing of the side face of a semiconductor chip 2 is carried out, and where the grinding of the rear face is carried out similarly, it has exposed. Furthermore, although not illustrated especially in the drawing 1 , the silicon-nitride layer 6 for raising the reliability as a semiconductor

device to the resin layer 3 maximum front face except the side face of these semiconductor chips 2, the rear face, and salient electrode 5 front face is considering as the insulating strengthening protective coat which prevents the reliability fall of the semiconductor device according [about 1 micrometer is comparatively formed at low temperature, and] to the moisture moisture absorption to the resin layer 3 of 200 degrees C - 250 degrees C by the plasma CVD method.

[0014] The junction technique to the printed wired board which shows that various package gestalt can be suited in the semiconductor device of the 1st example of this invention is explained based on drawing 3 . Drawing 3 is a cross section showing the junction technique to the printed wired board of the semiconductor device of the 1st example of this invention shown in drawing 1 . Direct face down bonding of the semiconductor device is carried out to the printed wired board 7 in which the foot pattern 8 was formed, and alloy junction of the salient electrode 5 of the Au bump 9 and the semiconductor chip 2 beforehand prepared on the foot pattern 8 is carried out by thermocompression bonding so that it may be shown in drawing 3 A. Moreover, in order to raise the reliability of the semiconductor device including this alloy junction section, the closure resin 10 of an epoxy system is closed for the periphery section of a semiconductor device by the potting method. As shown in drawing 3 B, the silicon system adhesives 11 of high temperature conductivity are applied to the rear face of the semiconductor device shown in drawing 3 A, aluminum alloy plate used as a heat sink 12 is stuck, and the thermolysis nature from a semiconductor device is raised positively. Drawing 3 C is the example of an about when the pitch of the salient electrode 5 formed in the semiconductor device is detailed, and it is the completely same technique as the junction technique of TAB tape of a usual tape career method, and the semiconductor chip 2. The 1st semiconductor device and TAB tape 13 of an example are joined through the salient electrode 5. It is the example which made the periphery section of the semiconductor device which is made to join the trailer of a lead of this TAB tape 13, and the foot pattern 8 on a printed wired board 7 using the joining method, and contains this soldered joint section close by the potting method by the closure resin 10 of an epoxy system like drawing 3 A and drawing 3 B. Drawing 3 D applies the silicon system adhesives 11 of high temperature conductivity to the semiconductor device rear face explained by drawing 3 C, sticks aluminum alloy plate used as a heat sink 12, and is raising the thermolysis nature from a semiconductor device.

[0015] Next, the 2nd example of this invention is explained based on drawing 4 . Drawing 4 A is the perspective diagram showing the semiconductor device of the 2nd example of this invention, and drawing 4 B shows the side elevation of drawing 4 A. As shown in drawing 4 A and drawing 4 B, the salient electrode 5 with two different heights is alternately formed around the semiconductor chip 2 on the semiconductor chip 2 thinly processed by rear-face grinding. And the low salient electrode 5 is formed in the array of the salient electrode 5 in which the high salient electrode 5 was formed in the outside at the array of the salient electrode 5 formed inside the semiconductor chip 2, and the resin layer 3 is formed in the shape of a card row so that the amount of vegetation may become 20 micrometers order. Thus, even if the salient electrode 5 on a semiconductor chip 2 serves as a detailed pitch by having constituted the semiconductor device, TAB bonding which the short-circuit during a contiguity lead seldom produces can be performed easily.

[0016] The 3rd example of this invention and the 4th example are explained below based on the drawing 5 and the drawing 6 . The drawing 5 and the drawing 6 are perspective diagrams showing the semiconductor device of the 3rd example and the 4th example, respectively. the 3rd example shown in drawing 5 is the solder for preventing the short-circuit by the solder bridge between the salient electrodes 5 which adjoined, when solder is used for the cementing material of the salient electrode 5 and the foot pattern 8 which is made to have formed the concavity 14 in the resin layer 3 of the periphery section of the salient electrode 5 which the semiconductor device was made to project, and shows this concavity 14 to drawing 3 A instead of the Au bump 9 -- the duty of a ball is given On the other hand, the 4th example shown in drawing 6 is an example for which the lateral part of the upper-limit section of the salient electrode 5 made to protrude on a semiconductor device and the circular cylinder flanks was exposed. A conductor pattern is continued and prepared [at a printed wired board 7] in length-like a conductor pattern (not shown) and a base the side face of a concave semiconductor device stowage (not shown) and the aforementioned semiconductor device stowage. The semiconductor device shown in the 4th example is contained to the semiconductor device stowage of a printed wired board 7. The reduction of the height at the time of the package to a

printed wired board 7 is aimed at at the same time it aims at the enhancement in a reliability at the time of a soldered joint, as the aforementioned conductor pattern is joined with solder for the upper-limit section and the circular cylinder flank of the salient electrode 5 of a semiconductor device.
[0017] The semiconductor device of this invention can be prevented from producing trauma of a crash of the semiconductor wafer 1, and the element side of a semiconductor chip 2 by forming the resin layer 3 in the front face of a semiconductor chip 2, as explained above. Moreover, a package height can be made small while making the two-dimensional electric flow path at the time of the package to a printed wired board 7 into the minimum.
[0018]
[Effect of the Invention] Even if the effect acquired by this invention processed the semiconductor wafer thinly by rear-face grinding, when the resin section formed on the semiconductor wafer functioned as a protection strengthening plate, while the semiconductor wafer crash at the time among rear-face grinding of a handling could be avoided, a handling of the semiconductor chip of the raise in basic wages status in an erector degree or a package process is lost, and the trauma to the element side of a semiconductor chip could also be avoided. Moreover, the semiconductor device of small and thin type can be formed now by the high-reliability which a two-dimensional electric flow path is [high-reliability] the minimum, and made thin easily resin thickness and semiconductor chip thickness by protruding the salient electrode which is made to become almost the same about the size of the resin section of the semiconductor device upper part, and the size of a semiconductor chip, and serves as an external end-connection child from the top of the resin section of the aforementioned semiconductor device upper part.

[Translation done.]

Effect

[Effect of the Invention] Even if the effect acquired by this invention processed the semiconductor wafer thinly by rear-face grinding, when the resin section formed on the semiconductor wafer functioned as a protection strengthening plate, while the semiconductor wafer crash at the time among rear-face grinding of a handling could be avoided, a handling of the semiconductor chip of the raise in basic wages status in an erector degree or a package process is lost, and the trauma to the element side of a semiconductor chip could also be avoided. Moreover, the semiconductor device of small and thin type can be formed now by the high-reliability which a two-dimensional electric flow path is [high-reliability] the minimum, and made thin easily resin thickness and semiconductor chip thickness by protruding the salient electrode which is made to become almost the same about the size of the resin section of the semiconductor device upper part, and the size of a semiconductor chip, and serves as an external end-connection child from the top of the resin section of the aforementioned semiconductor device upper part.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The perspective diagram showing the semiconductor device of the 1st example of this invention.
[Drawing 2] The cross section explaining the manufacture technique of the semiconductor device of the 1st example of this invention.
[Drawing 3] The cross section showing the junction technique to the printed wired board of the semiconductor device of the 1st example of this invention.
[Drawing 4] The perspective diagram and cross section showing the semiconductor device of the 2nd example of this invention.
[Drawing 5] The perspective diagram showing the semiconductor device of the 3rd example of this invention.
[Drawing 6] It is the perspective diagram showing the semiconductor device of the 4th example of this invention.
[Description of Notations]
1 Semiconductor Wafer
2 Semiconductor Chip
3 Polyimide-Resin Layer
4 Scribe Line
5 Salient Electrode
6 Silicon-Nitride Layer
7 Printed Wired Board
8 Foot Pattern
9 Au Bump
10 Closure Resin
11 Silicon System Adhesives
12 Heat Sink
13 TAB Tape

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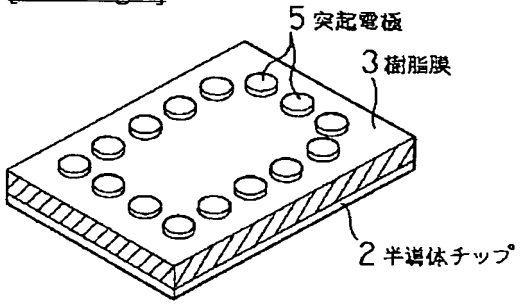
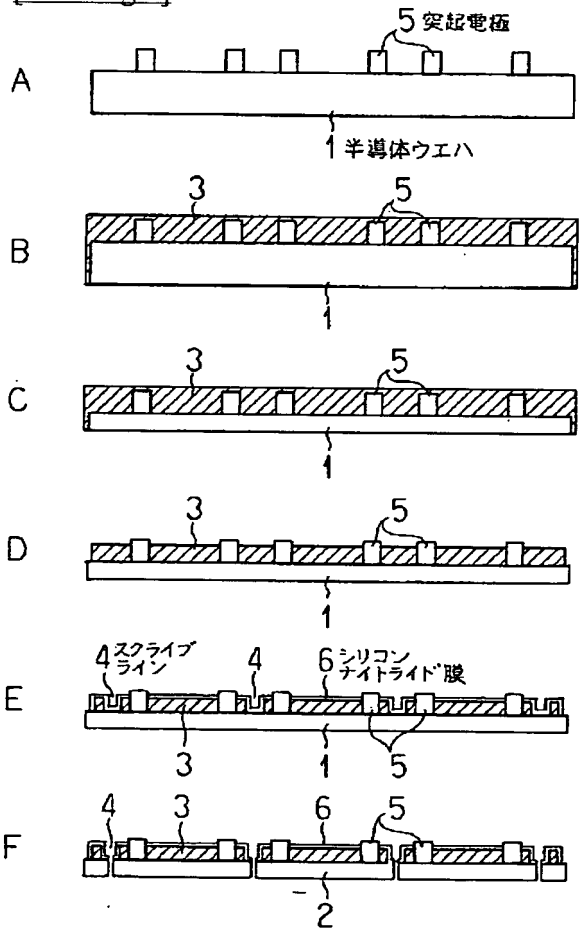
DRAWINGS

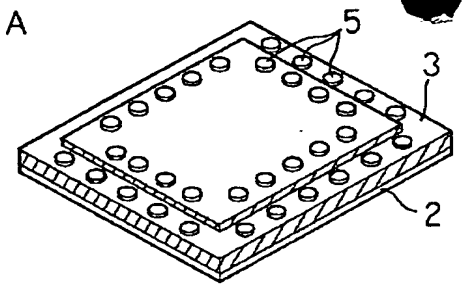
[Drawing 1]

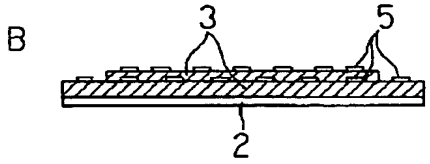


[Drawing 2]

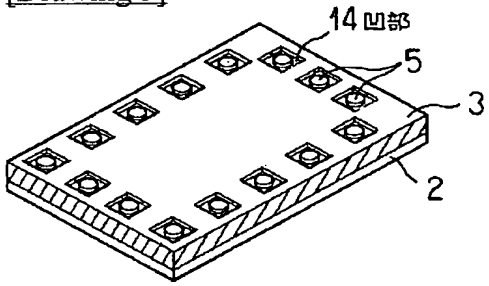


[Drawing 4]

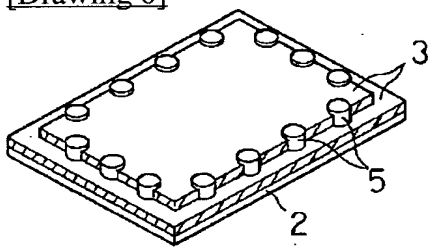




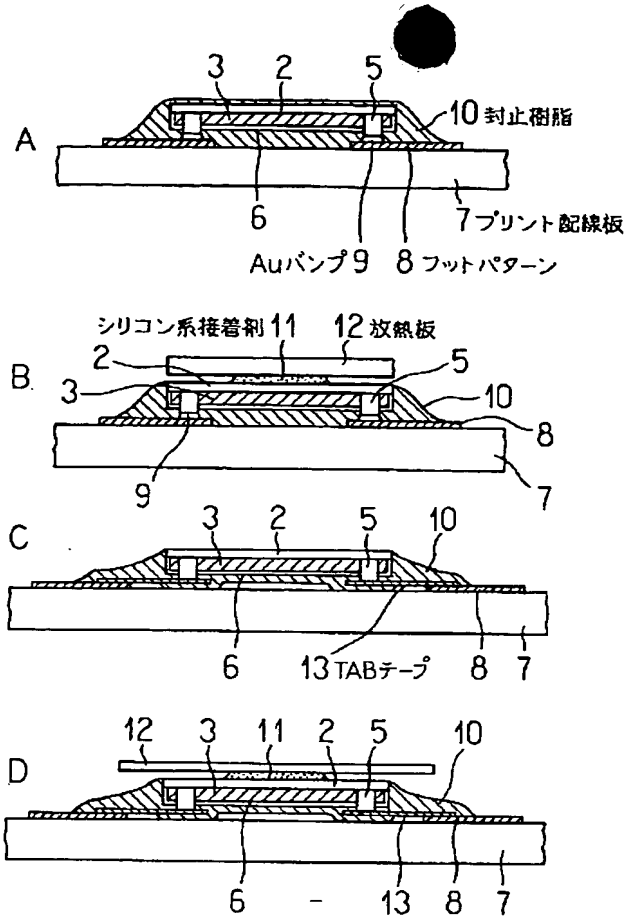
[Drawing 5]



[Drawing 6]



[Drawing 3]



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21/304	３２１	Ｂ 8831－4M		
21/78		Ｌ 8617－4M		
		9168－4M	Ｈ０１Ｌ 21/ 92	Ｂ
		7352－4M	23/ 12	Ｌ

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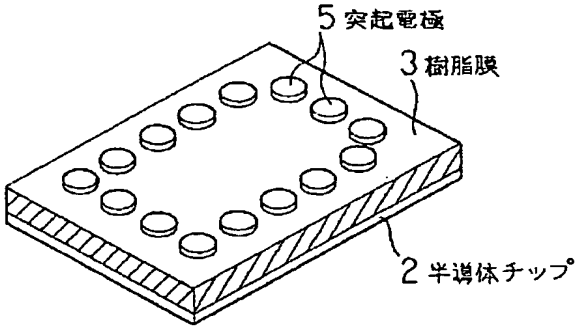
(54)【発明の名称】　半導体装置

(57)【要約】

【目的】半導体チップそのものの厚みを半導体ウエハの大きさによらず薄くさせながら、製造工程における半導体チップの取り扱い作業性を向上させ、かつ、小型、薄型の半導体装置を得る。

【構成】樹脂膜３を保護強化板としながら半導体ウエハ１を薄くし、かつ、半導体チップ２上の樹脂膜３から突起電極５を突出させて外部接続端子とし、樹脂膜３の大きさを半導体チップ２と同一になるように切断する。

【効果】高信頼性で取り扱い容易な、小型、薄型の半導体装置が得られる。



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【特許請求の範囲】

【請求項１】　半導体チップの側面および下面が露出し、前記半導体チップ上面にこれとほぼ同一の大きさを有する樹脂部が形成され、前記樹脂部の上面から突起電極が突設されていることを特徴とする半導体装置。

【請求項２】　前記樹脂部の最表面の主部に絶縁保護強化膜が形成されていることを特徴とする特許請求項１に記載の半導体装置。

【請求項３】　前記突起電極が埋設された樹脂部を保護強化板としながら半導体ウエハ裏面部を除去させたことを特徴とする特許請求項１に記載の半導体装置の製造方法。

【請求項４】　前記樹脂部から突起電極先端部および半導体ウエハの切断領域を露出させた後に、樹脂部最表面および切断領域表面に絶縁保護強化膜を形成し、切断領域を切断することを特徴とする特許請求項１に記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体チップのパッド電極膜上に形成された突起電極先端部を外部接続端子となす半導体装置に関する。

【０００２】

【従来の技術】一般にパターン形成が完了した半導体ウエハは裏面研削法を用いて所定の厚みに研削される。この裏面研削法は、保護フィルムとなる塩化ビニールなどを基材とする軟質性フィルムを半導体ウエハのパターン面に貼り付け、軟質フィルム上から半導体ウエハを均一に加圧して回転させながら、ダイヤモンド粒が樹脂中に練入された粒石により半導体ウエハ裏面を研削、除去するものである。

【０００３】そして研削された半導体ウエハのスクライブラインを切断して個々の半導体チップに分割し、半導体チップと外部端子リードとをボンディングワイヤあるいはＴＡＢリードなどを介して相互に電気的に接合させ、樹脂封止後に外部端子リードを加工形成させるというものが一般的な技術であった。

【０００４】また、半導体ウエハ上にＡｕバンプなどの突起電極を形成させるには、前記裏面研削法による半導体ウエハ裏面を研削し、除去する前もしくは後に、Ｃｒなどのバリア金属膜を形成して、Ａｕ電解メッキ法によりＡｕバンプを選択的に形成させていた。

【０００５】

【発明が解決しようとする課題】半導体装置は、コンピュータ、ワークステーション、パーソナルコンピュータ、ワードプロセッサ、携帯電話、小型携帯カムコーダなどのあらゆる機器に多量に搭載されている。近年、これらの機器の小型化、軽量化の進展は著しく、また、今後これらの機器の小型化、軽量化そして高性能化、高機能化はさらに進むことから、これらの機器に搭載される

2

半導体装置の小型化、薄形化、高信頼性化への要求は、半導体素子の高集積化、高機能化という要求と合わせて加速度的に増大していくものと予測される。しかしながら、半導体ウエハの大口径化の進展にともない従来の裏面研削法による半導体ウエハ厚の加工には、ハンドリング時もしくは研削時の半導体ウエハの破損防止という制約により厚みを薄くすることに限界が生じ、この結果、半導体装置に収納する半導体チップが厚くなり、半導体装置の薄形化ひいては機器の薄形化を阻害する要因となっている。さらに、半導体ウエハは裏面研削時のＡｕバンプへの荷重集中による半導体ウエハの破損を回避するために、Ａｕバンプの形成を裏面研削後に行っているのが一般的であり、Ａｕバンプを形成した後に裏面研削を行うことは、荷重の局部集中による半導体ウエハの破損を回避することを考慮すると、非常な困難さを伴うおそれがあった。

【０００６】一方、機器内での半導体装置が占める実装面積は、半導体素子の高集積化、高機能化にともない増大する方向にあり、特に、従来の半導体装置の内側はボンディングワイヤ、インナーリードなどの電気的導通経路を必要とし、かつ、半導体装置の外側には接合を得るためのアウターリードを必要とするために本質的に実装面積は大きくなり、さらには、樹脂厚みと半導体チップ厚みからなる実装高さも高くなり、これらのことが半導体装置の小型化、軽量化を阻害し、ひいては、機器の小型化、軽量化を阻害する要因となっていた。

【０００７】さらに、研削後に分割される半導体チップの素子面は外部からのわずかな力により簡単に損傷を受けやすく、組立工程や実装工程における半導体チップのハンドリングや装置条件の設定には細心の注意が必要であった。

【０００８】本発明は、半導体ウエハを裏面研削により薄く加工しても半導体ウエハ破損が生じないようにすることと同時に半導体チップの素子面への損傷が生じないようにすること、そして、２次元的な電気的導通経路を最小にして実装面積を小さくし、かつ、樹脂厚みおよび半導体チップ厚みを最小にして実装高さを小さくすることを目的としている。

【０００９】

【課題を解決するための手段】本発明の半導体装置は、前述のような課題を解決するものであって、その概要を説明すればつぎの通りである。すなわち、外部接続端子となる突起電極を埋設した樹脂部を保護強化板としながら半導体ウエハ裏面部を研削して半導体ウエハを薄くし、この樹脂部から突起電極先端部および半導体ウエハのスクライブラインを露出させた後に樹脂部最表面の主部およびスクライブライン部表面に絶縁保護強化膜を形成してからスクライブラインを切断して半導体装置を構成させ、そして、この半導体装置上部の樹脂部の上面から突設された突起電極が外部接続端子として電気的かつ

機械的接合を得るように構成したものである。

【0010】

【作用】前述の手段によれば、半導体ウエハを裏面研削により薄く加工しても半導体ウエハ上に形成された樹脂部が保護強化板として機能するために、裏面研削中およびハンドリング時の半導体ウエハ破損を回避できると同時に、組立工程や実装工程におけるベア状態での半導体チップのハンドリングはなくなり、半導体チップの素子面への損傷も回避できる。また、半導体装置上部の樹脂部の大きさと半導体チップの大きさをほぼ同一となるようにし、前記半導体装置の上部に形成された樹脂部の上面から外部接続端子となる突起電極を突設することにより、容易に2次元的な電気的導通経路を最小にし、かつ、樹脂厚みおよび半導体チップ厚みを薄くさせた小型、薄型の半導体装置を形成することができる。

【0011】

【実施例】本発明の第1の実施例を図1および図2にもとづいて説明する。図1は本発明の第1の実施例の半導体装置を示す斜視図であり、図2は第1の実施例の半導体装置の製造方法について説明する断面図である。図1は表面に樹脂膜3および突起電極5を形成した半導体ウエハ1を個々の半導体チップ2の大きさに切断した状態を示しており、切断前において表面に樹脂膜3を形成した状態で半導体ウエハ1の裏面を裏面研削法を用いて鏡面状に研削を行って、半導体ウエハ1の厚みを薄く加工した後、スクライブライン4をダイシングブレードを用いて切断している。この半導体ウエハ1の裏面の研削は、裏面研削前に半導体ウエハ1の表面に樹脂膜3を形成させることにより、樹脂膜3を保護強化板として機能させ、6インチ径の半導体ウエハ1であればウエハプロセス加工時の厚みが約0．6mmのものが裏面研削法により0．35mm～0．4mm程度まで半導体ウエハ1の厚みを薄く加工でき、8インチ径の半導体ウエハ1であってもウエハプロセス加工時の厚みが0．7mm程度のものが同様に0．4mm～0．5mm程度まで半導体ウエハ1の厚みを薄く加工できる。このことにより、半導体ウエハ1の厚み、すなわち、半導体ウエハ1の大きさ如何に関わらず半導体ウエハ1の厚みを薄く加工することができる。ここで、この樹脂膜3を形成する樹脂材料には、例えば低応力、高耐熱性を有するポリイミド樹脂を用いており、樹脂部の形成方法には一般によく用いられているポリイミド樹脂をスピンコーティングした後に熱硬化させる方法を用いている。また所定の樹脂膜厚を得るためには、スピンコーティングを繰り返すことにより容易に得られる。なお、半導体ウエハ1の表面に形成される樹脂膜3の樹脂材料としては、前述のようなポリイミド樹脂の代わりに、低応力、低収縮性を有するエポキシ系の樹脂を用いることも可能であり、所定の樹脂膜3の厚みはスキージ印刷法を用いることにより容易に得ることができ、この結果、樹脂膜3の保護強化板としての機能はさらに向上することになる。

【0012】本発明の第1の実施例の半導体装置の製造方法を図2にもとづいて説明する。まず、第1の工程では図2Aに示すように、パターンが形成された0．6mm程度の厚みを有する半導体ウエハ1の電極パッド上に、クロム薄膜を介して電解メッキ法により選択的にAuメッキを施し、円柱状の突起電極5を約100μmの高さで形成する。つぎに、第2の工程では図2Bに示すように、半導体ウエハ1上に突起電極5の上端部を覆う程度の厚みで樹脂膜3を形成する。そして、第3の工程では図2Cに示すように、この樹脂膜3を保護強化板および接着剤として半導体ウエハ1の裏面を裏面研削法により研削し半導体ウエハ1の厚みを0．4mm程度となるように薄く加工する。第4の工程では図2Dに示すように、半導体ウエハ1の上部に設けられた樹脂膜3の上面を軽くエッチングし、突起電極5の上端部を露出させる。　第5の工程では図2Eに示すように、ダイシングブレードにてスクライブライン4の樹脂膜3を削り取り、高温乾燥後、プラズマCVD法によりシリコンナイトライド膜6を突起電極5の上端部を除いて選択的に形成させる。最後に、第6の工程では図2Fに示すように、ダイシング用粘着性テープ（図示せず）にこの半導体ウエハ1を貼り、スクライブライン4で半導体ウエハ1を完全にダイシングブレードにて削りとり、1個1個の半導体チップ2に分離する。なお、スクライブライン4の樹脂膜3を取り除くためには、第5の工程で説明したような物理的な方法だけではなく、化学的エッチングによる方法も可能である。一方、シリコンナイトライド膜6の形成は、絶縁強化保護としての機能は若干低下するが、樹脂膜3の軽いエッチング直後に行うことも可能である。

【0013】さらに、図1において前述のように個々の半導体チップ2の大きさに切り出された半導体装置は、既に説明した通り裏面研削を施されて薄くなった半導体チップ2の上面に樹脂膜3が形成されており、この樹脂膜3の上面からは半導体チップ2のパッド電極に対して垂直に形成された円柱状の突起電極5の先端部が突出しており、その突起電極5は電解メッキ法を用いて形成されたAu電極であり、その高さは80μm～100μmである。ただし、この突起電極5の形状は、円柱状であっても良いし、角柱状であっても良い。一方、この突起電極5の突出量は、突起電極5の高さ、樹脂膜3の厚み、そして、接合安定性から決定され、第1の実施例では20μm程度を突出させている。また、第1の実施例では、半導体チップ2の側面がダイシングされた状態で露出しており、同様にその裏面が研削された状態で露出している。さらに、図1では特に図示してはいないが、これら半導体チップ2の側面、裏面および突起電極5表面を除いた樹脂膜3最表面には半導体装置としての信頼性を高めるためのシリコンナイトライド膜6がプラズマ

5

ＣＶＤ法により２００℃～２５０℃の比較的低温で１μｍ程度形成され、樹脂膜３への水分吸湿による半導体装置の信頼性低下を防ぐ絶縁強化保護膜としている。

【００１４】本発明の第１の実施例の半導体装置を種々の実装形態に適合できることを示すプリント配線板への接合方法を図３にもとづいて説明する。図３は、図１に示した本発明の第１の実施例の半導体装置のプリント配線板への接合方法を示す断面図である。図３Ａにしめすように、フットパターン８が形成されたプリント配線板７へ半導体装置が直接フェイスダウンボンディングされており、フットパターン８上に予め設けられたＡｕバンプ９と半導体チップ２の突起電極５が熱圧着により合金接合されている。またこの合金接合部を含めた半導体装置の信頼性を高めるために、半導体装置の周縁部をエポキシ系の封止樹脂１０をポッティング法で封止している。図３Ｂに示すように、図３Ａに示した半導体装置の裏面に高熱伝導性のシリコン系接着剤１１を塗布し、放熱板１２となるＡｌ合金板を貼付け、半導体装置からの放熱性を積極的に向上させている。図３Ｃは、半導体装置に形成された突起電極５のピッチが微細な場合についての実施例であり、通常のテープキャリア方式のＴＡＢテープと半導体チップ２との接合方法と全く同一な方法で、第１の実施例の半導体装置とＴＡＢテープ１３とを突起電極５を介して接合させ、そして、このＴＡＢテープ１３のリードの終端部とプリント配線板７上のフットパターン８とを半田接合法を用いて接合させ、この半田接合部を含む半導体装置の周縁部を図３Ａ，図３Ｂと同様にエポキシ系の封止樹脂１０でポッティング法により封止させた例である。図３Ｄは、図３Ｃで説明した半導体装置裏面に高熱伝導性のシリコン系接着剤１１を塗布し、放熱板１２となるＡｌ合金板を貼り付け、半導体装置からの放熱性を向上させている。

【００１５】次に、本発明の第２の実施例を図４にもとづいて説明する。図４Ａは、本発明の第２の実施例の半導体装置を示す斜視図であり、図４Ｂは図４Ａの側面図を示している。図４Ａ、図４Ｂに示すように、裏面研削により薄く加工された半導体チップ２上に２つの異なる高さを有した突起電極５が千鳥状に半導体チップ２の周囲に形成されている。そして、半導体チップ２の内側に形成された突起電極５の配列には高い突起電極５が、その外側に形成された突起電極５の配列には低い突起電極５が形成され、突出量が２０μｍ前後となるように樹脂膜３が段状に形成されている。このように半導体装置を構成したことにより、半導体チップ２上の突起電極５が微細ピッチとなっても、隣接リード間のショートが生じにくいＴＡＢボンディングが容易に行えるようになる。

【００１６】つぎに本発明の第３の実施例および第４の実施例を、図５および図６にもとづいて説明する。図５および図６は、それぞれ第３の実施例および第４の実施例の半導体装置を示す斜視図である。図５に示す第３の

6

実施例は、半導体装置に突出させた突起電極５の周囲部の樹脂膜３に凹部１４を形成させてあり、この凹部１４を、図３Ａに示す突起電極５とフットパターン８との接合材料にＡｕバンプ９の代わりに半田を用いたときに、隣接した突起電極５間での半田ブリッジによるショートを防ぐための半田だまりの役目を持たせている。一方、図６に示す第４の実施例は、半導体装置に突設させた突起電極５の上端部と円柱側部のうちの外側部を露出させた例であり、プリント配線板７に凹状の半導体装置収納部（図示せず）と前記半導体装置収納部の側面に縦状の導体パターン（図示せず）と底面に導体パターンを連続して設け、第４の実施例に示した半導体装置をプリント配線板７の半導体装置収納部に収納し、半導体装置の突起電極５の上端部と円柱側部とを前記導体パターンとを半田接合させるようにして半田接合時の信頼性向上をはかると同時に、プリント配線板７への実装時の高さの低減をはかっている。

【００１７】以上説明してきたように、本発明の半導体装置は半導体チップ２の表面に樹脂膜３を形成することにより、半導体ウエハ１の破損、半導体チップ２の素子面の損傷を生じないようにすることができる。また、プリント配線板７への実装時の２次元的な電気導通経路を最小にすると同時に実装高さを小さくすることができる。

【００１８】

【発明の効果】本発明により得られる効果は、半導体ウエハを裏面研削により薄く加工しても半導体ウエハ上に形成された樹脂部が保護強化板として機能することにより裏面研削中およびハンドリング時の半導体ウエハ破損は回避できるようになったと同時に、組立工程や実装工程におけるベア状態の半導体チップのハンドリングがなくなり半導体チップの素子面への損傷も回避できるようになった。また、半導体装置上部の樹脂部の大きさと半導体チップの大きさをほぼ同一となるようにし、前記半導体装置上部の樹脂部の上面から外部接続端子となる突起電極を突設することにより、容易に、２次元的な電気的導通経路が最小で、かつ、樹脂厚みおよび半導体チップ厚みを薄くさせた高信頼性で小型かつ薄形の半導体装置を形成できるようになった。

【図面の簡単な説明】

【図１】本発明の第１の実施例の半導体装置を示す斜視図。

【図２】本発明の第１の実施例の半導体装置の製造方法について説明する断面図。

【図３】本発明の第１の実施例の半導体装置のプリント配線板への接合方法を示す断面図。

【図４】本発明の第２の実施例の半導体装置を示す斜視図および断面図。

【図５】本発明の第３の実施例の半導体装置を示す斜視図。

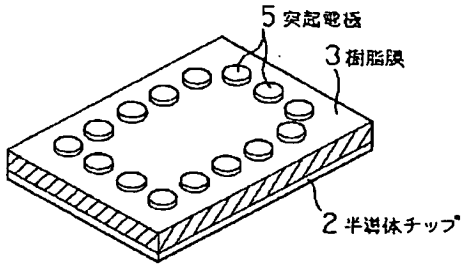
7　　8

【図6】本発明の第4の実施例の半導体装置を示す斜視図である。

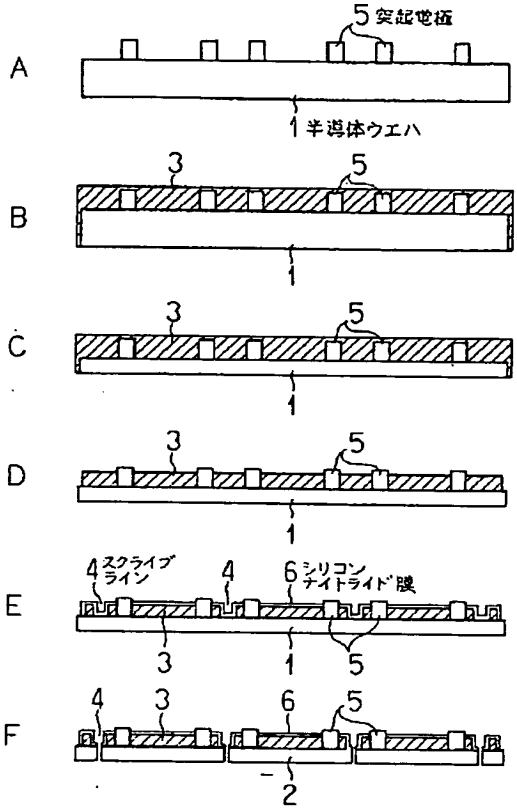
【符号の説明】

1　半導体ウエハ
2　半導体チップ
3　ポリイミド樹脂膜
4　スクライブライン
5　突起電極
＊6　シリコンナイトライド膜
7　プリント配線板
8　フットパターン
9　Auバンプ
10　封止樹脂
11　シリコン系接着剤
12　放熱板
＊　13　TABテープ

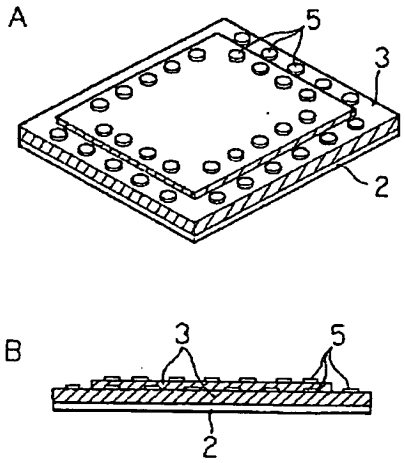
【図1】



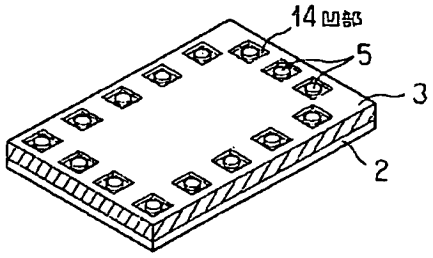
【図2】



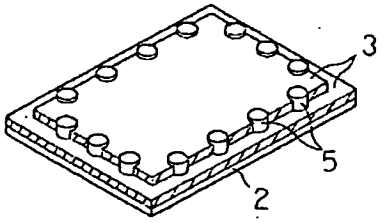
【図4】



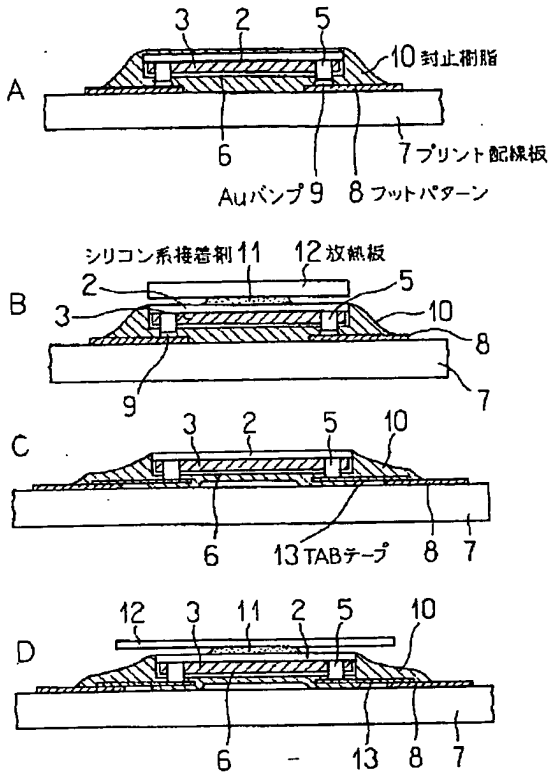
【図5】



【図6】



【図3】



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